

Introduction

The ISL8107 is a single-phase PWM controller that operates from 9V to 75V bias supply voltage. The PWM controller drives an external high-side N-Channel MOSFET in a non-synchronous buck converter topology. The ISL8107 features input voltage feed-forward compensation and overcurrent protection, etc. For a more detailed description of the ISL8107 functionality, refer to the ISL8107 Data Sheet <http://www.intersil.com/data/fn/fn6605.pdf>.

The ISL8107EVAL1Z Reference Design

The ISL8107EVAL1Z evaluation board is designed to meet the output voltage and current specifications shown in Table 1. Schematic, bill of materials, and layout plots are included.

TABLE 1. ISL8107EVAL1Z DESIGN PARAMETERS

PARAMETER	MIN	TYP	MAX
Input Voltage (V_{IN})	9V	48V	75V
Output Voltage (V_{OUT})		5V	
Output Voltage Ripple		20mV	
Continuous Load Current	0.1		8A
Switching Frequency		200kHz	

Quick Start Evaluation

Figure 1 shows a photograph of the ISL8107EVAL1Z board.



FIGURE 1. ISL8107EVAL1Z

Circuit Setup

The input supply of the power stage can be connected to the terminals J1 (V_{IN}) and J2 (PGND). For single supply application, the ISL8107's bias supply can be tied to V_{IN} through J5 with shunt between pins 2 and 3. When using separate supplies, provide the ISL8107 bias voltage through P1 (VBIAS) with J5's shunt between pins 1 and 2. The load can be connected to terminal J3 (V_{OUT}) and J4 (PGND). TP3 and TP4 can be used for DMM to measure the output voltage. Enabling and disabling the controller can be done through the toggle switch, SW1.

ISL8107EVAL1Z Performance

Start-Up

Figure 2 shows the start-up waveforms of the ISL8107EVAL1Z. Upon the VCC and VFF exceeding their rising POR thresholds, the ISL8107 provides initially $2\mu\text{A}$ to charge the soft-start capacitor, C_{SS} , connected to the ENSS pin. If the voltage at this pin is allowed to rise (the toggle switch, SW1, at ON position), the voltage on ENSS pin will ramp-up with at a slope determined by the $2\mu\text{A}$ current and the value of the soft-start capacitor. When the voltage at ENSS reaches 0.77V, the oscillator circuit is active, and generates sawtooth waveform. At the same time, the soft-start current is increased to $33\mu\text{A}$; the ENSS voltage then ramps up at a faster rate. The UGATE starts switching when the ENSS voltage reaches 1.4V (Typ).

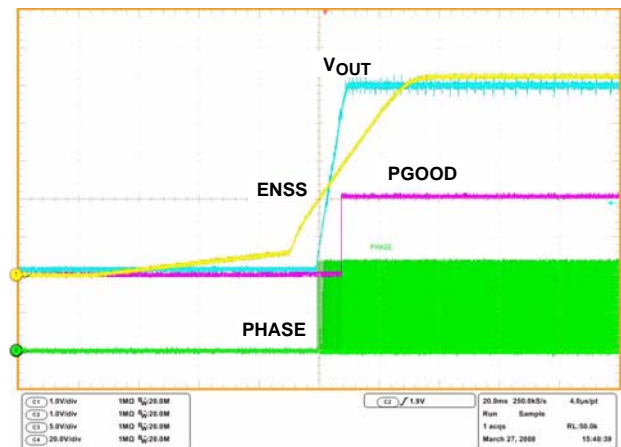


FIGURE 2. START-UP WAVEFORMS

Output Voltage Ripple

Figure 3 shows the ripple voltage on the output of the regulator at 8A load current.

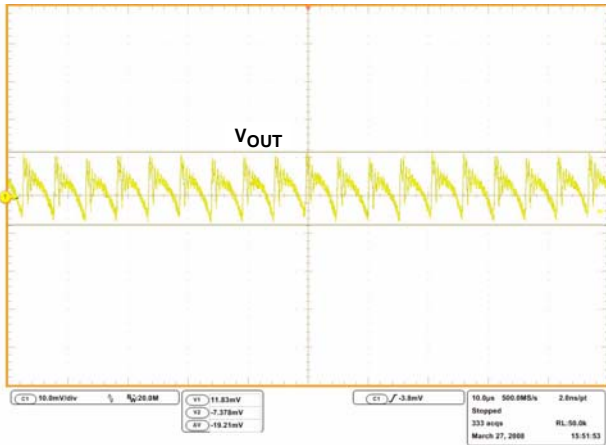


FIGURE 3. OUTPUT VOLTAGE RIPPLE @ $I_{OUT} = 8A$ (20MHz BW)

Transient Responses

Figures 4, 5, and 6 show the response of the output when subjected to transient loading from 4A to 8A at $1A/\mu s$ (within continuous conduction mode).

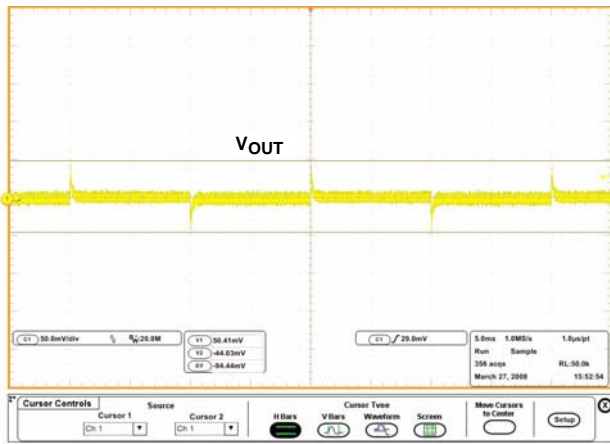


FIGURE 4. OUTPUT TRANSIENT

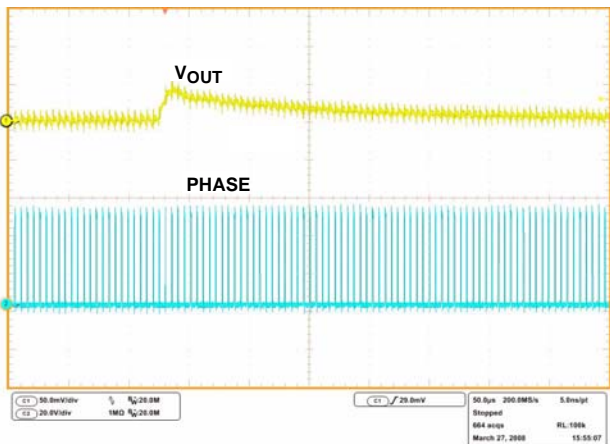


FIGURE 5. OUTPUT TRANSIENT

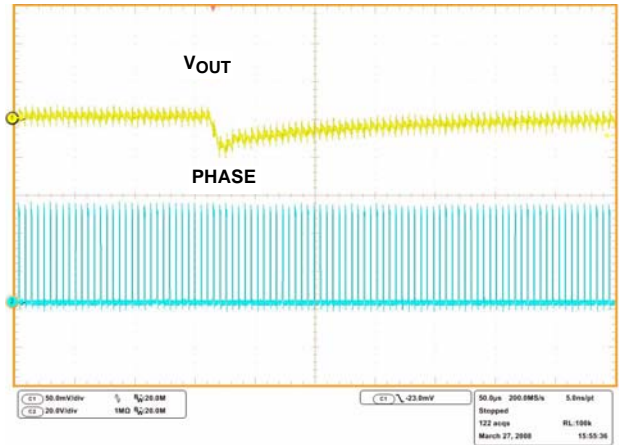


FIGURE 6. OUTPUT TRANSIENT

Figure 7 shows the response of the output when subjected to transient loading from 0.1A to 8A at $1A/\mu s$ (transition between continuous conduction mode and discontinuous conduction mode).

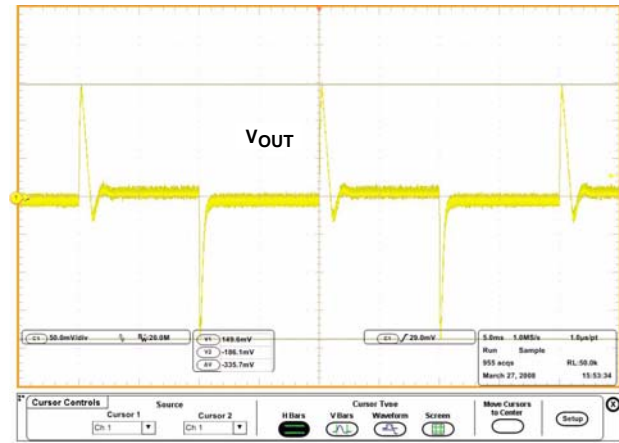


FIGURE 7. OUTPUT TRANSIENT

Efficiency

The efficiency of the evaluation board with various input voltage and 5V output voltage is shown in Figures 8 and 9.

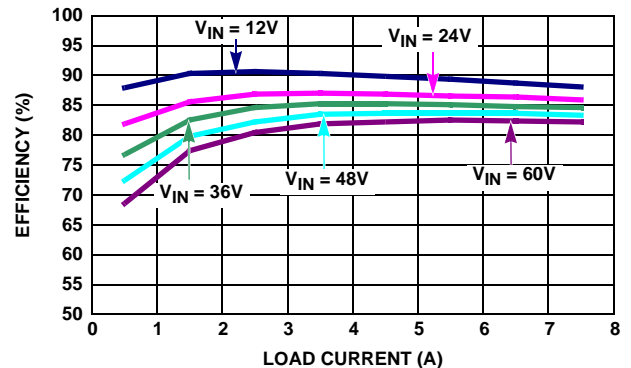


FIGURE 8. CONVERTER EFFICIENCY ($V_{OUT} = 5V$)

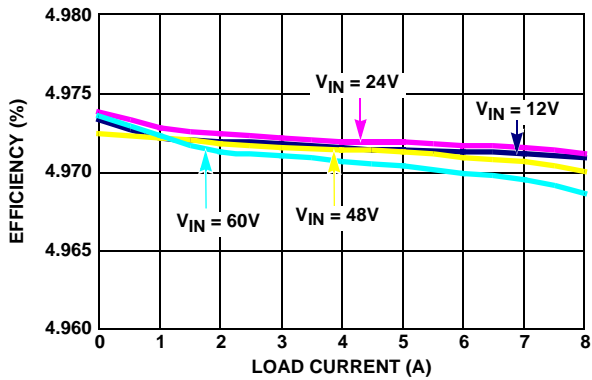


FIGURE 9. LINE REGULATION FOR $V_{OUT} = 5V$

With resistor R_4 changed to 1.3k, the output voltage is set to 12V. The efficiency of the evaluation board is shown in Figure 10.

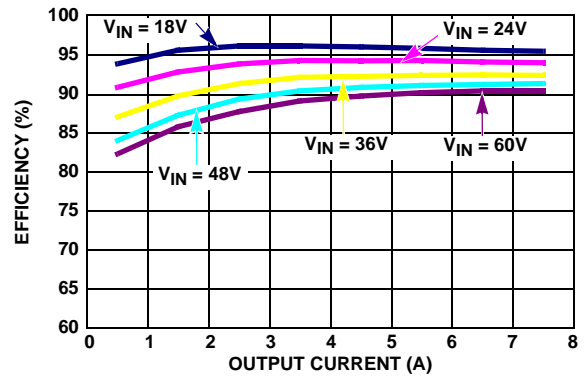
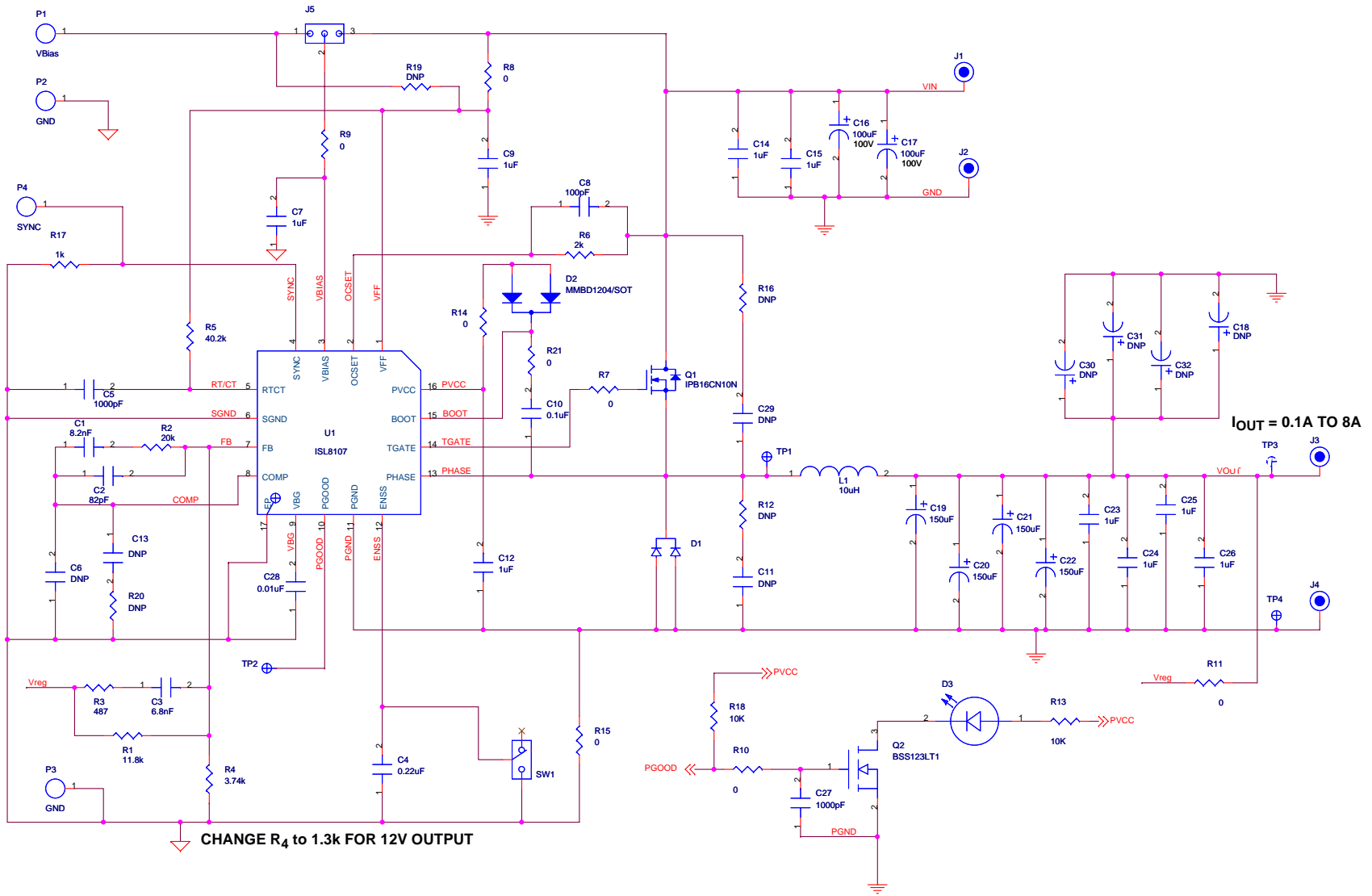


FIGURE 10. CONVERTER EFFICIENCY ($V_{OUT} = 12V$)

Schematic



Application Note 1402

Bill of Materials

REFERENCE	QTY	PART NUMBER	DESCRIPTION	PACKAGE	VENDOR
U1	1	ISL8107IRZ	Single PWM Controller	16 Ld QFN	Intersil
Q1	1	IPB16CN10N G	100V N-Channel MOSFET	D2PAK	Infineon
Q2	1	BSS123LT1G	N-Channel MOSFET, 0.17A	SOT-23	On Semi.
D1	1	STPS20H100CG	100V Schottky Diode Rectifier	D2PAK	ST Micro.
D2	1	MMBD1204	100V Ultrafast Diode	SOT-23	Fairchild
D3	1	597-3311	LED Green	SMD1206	DIALIGHT
L1	1	IHLP5050FDER100M01	10 μ H Power Inductor	SMD 12.9x13.2	Vishay
CAPACITORS					
C1	1		8200pF, 50V, X7R, 10%, Ceramic Capacitor	0603	Various
C2	1		82pF, 50V, COG, 10%, Ceramic Capacitor	0603	Various
C3	1		6800pF, 50V, X7R, 10%, Ceramic Capacitor	0603	Various
C4	1		0.22 μ F, 16V, X7R, 10%, Ceramic Capacitor	0603	Various
C5	1	GRM2195C2A102JA01D	1000pF, 100V, COG, 5%, Ceramic Capacitor	0805	Murata
C7, C9, C14, C15, C23 through C26	8		1 μ F, 100V, X7R, 10%, Ceramic Capacitor	1210	Various
C8	1		100pF, 50V, COG, 10%, Ceramic Capacitor	0603	Various
C10	1		0.1 μ F, 50V, X7R, 10%, Ceramic Capacitor	0603	Various
C12	1		1 μ F, 25V, X5R, 10%, Ceramic Capacitor	0805	Various
C16, C17	2	100ME100PX	100 μ F, 100V, Aluminum Electrolytic Capacitor	RAD 12.5x20	Sanyo
C19 through C22	4	20SEQP150M	150 μ F, 20V, OSCON Capacitor	RAD 10x13	Sanyo
C27	1		1000pF, 50V, X7R, 10%, Ceramic Capacitor	0603	Various
C28	1		0.01 μ F, 50V, X7R, 10%, Ceramic Capacitor	0603	Various
C6, C11, C13, C18, C29 through C32	0	DNP			
RESISTORS					
R1	1		Resistor, 11.8k Ω , 1%, 1/10W	0603	Various
R2	1		Resistor, 20k Ω , 1%, 1/10W	0603	Various
R3	1		Resistor, 487 Ω , 1%, 1/10W	0603	Various
R4	1		Resistor, 3.74k Ω , 1%, 1/10W	0603	Various
R5	1		Resistor, 40.2k Ω , 1%, 1/10W	0603	Various
R6	1		Resistor, 2k Ω , 1%, 1/10W	0603	Various
R7 through R11, R14, R15, R21	8		0 Ω Resistor, 1/10W	0603	Various
R13, R188	2		Resistor, 10k Ω , 5%, 1/10W	0603	Various
R17	1		Resistor, 1k Ω , 1%, 1/10W	0603	Various
R12, R16, R19, R20	0	DNP			
OTHERS					
J1, J3	2	111-0702-001	Blinding Post, Red		Johnson
J2, J4	2	111-0703-001	Blinding Post, Black		Johnson
J5	1	68000-236-1X3	Connector Header		BERG/FCI
SW1	1	GT11MSCKE	SMD Toggle Switch		C&K
P1 through P4	4	1514-2	Turret Post		Keystone

ISL8107EVAL1Z Layout

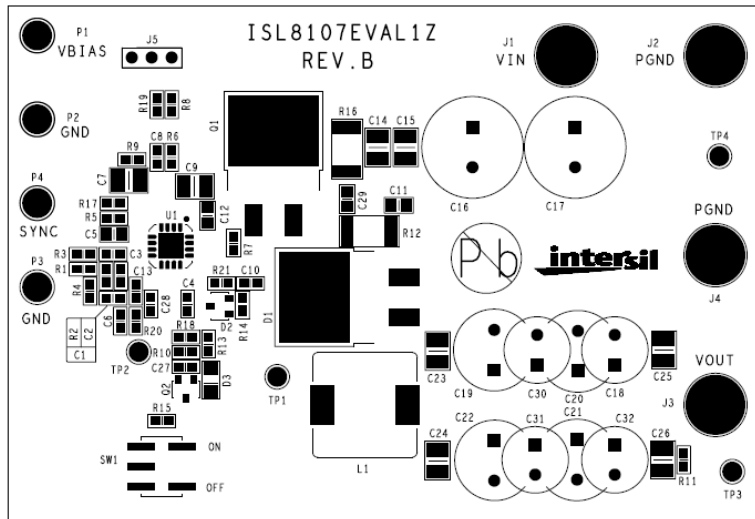


FIGURE 11. TOP SILK SCREEN

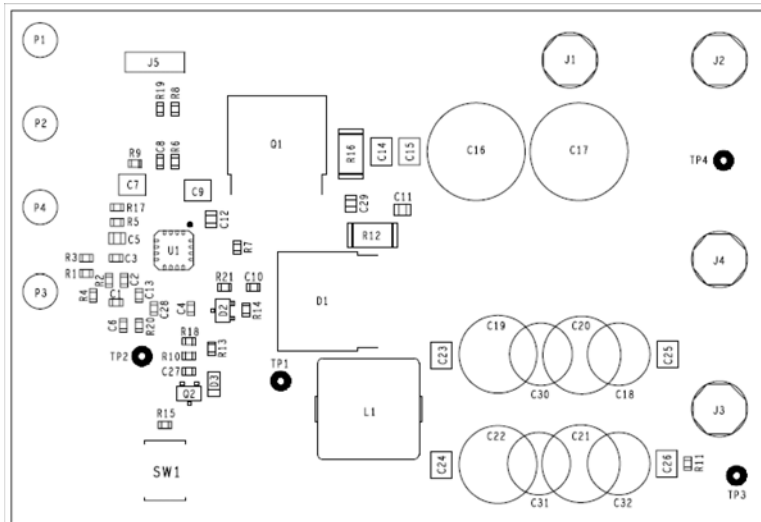


FIGURE 12. TOP ASSEMBLY

ISL8107EVAL1Z Layout (Continued)

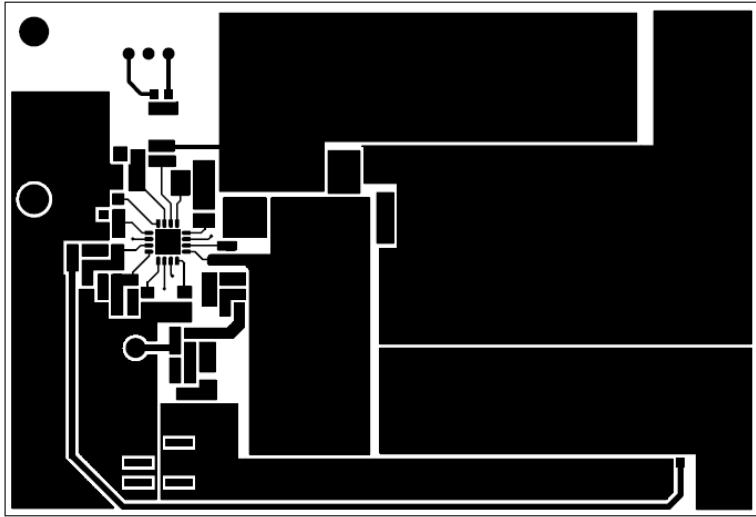


FIGURE 13. TOP LAYER

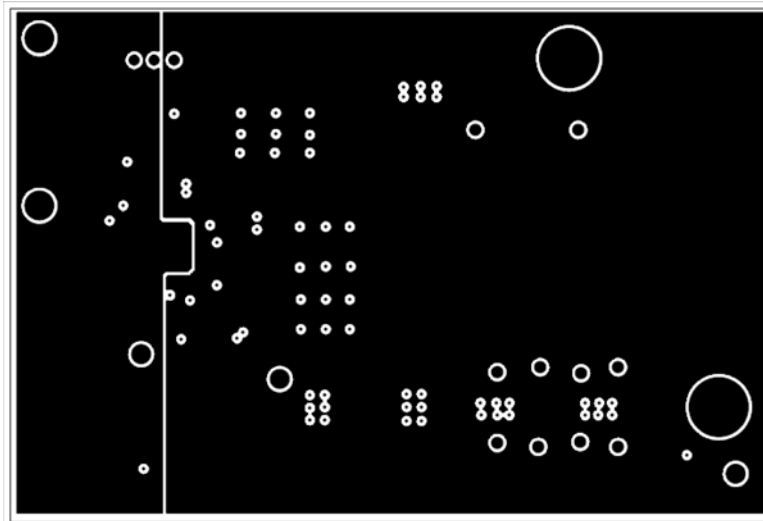


FIGURE 14. LAYER 2

ISL8107EVAL1Z Layout (Continued)

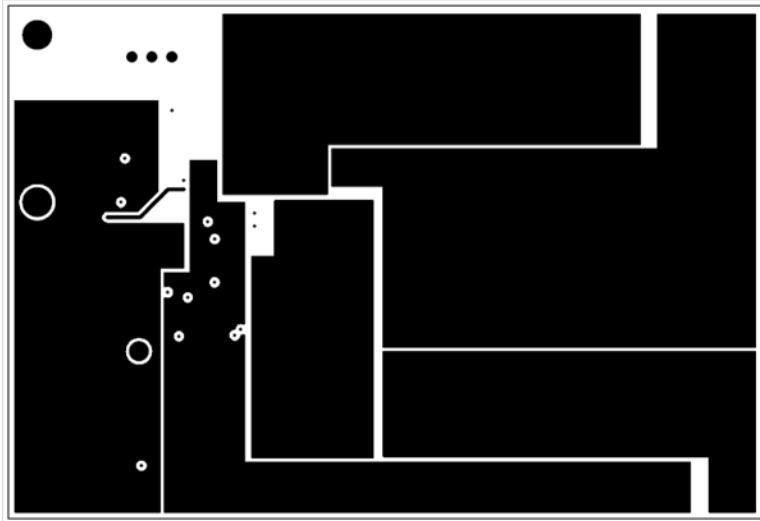


FIGURE 15. LAYER 3

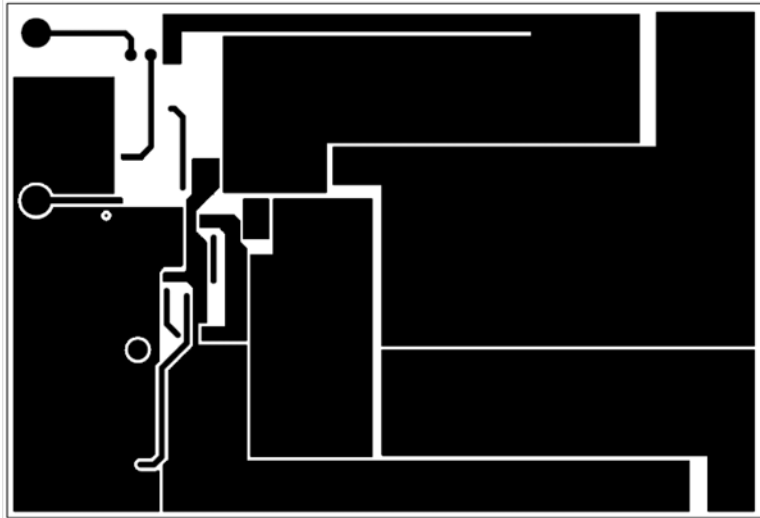


FIGURE 16. BOTTOM LAYER

ISL8107EVAL1Z Layout (Continued)

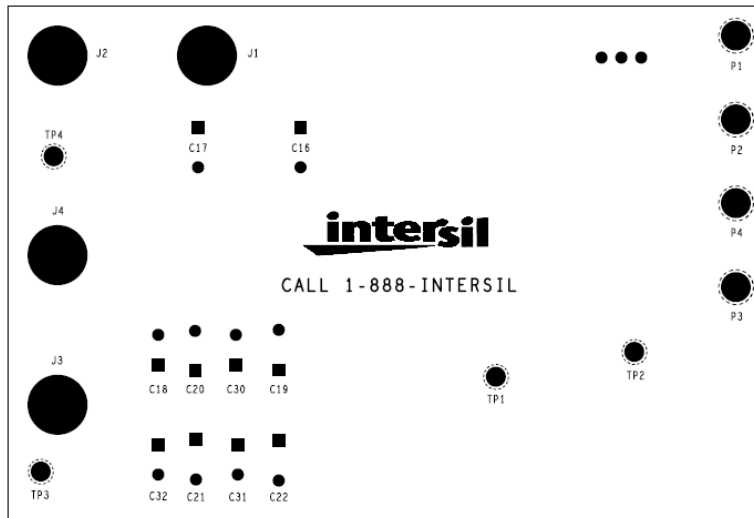


FIGURE 17. BOTTOM SILK SCREEN

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